Such an apparatus and such a method are disclosed in WO 99/34520, corresponding to U.S. Patent NO. 6,115,436 to Ramesh et al. (hereinafter "Ramesh").

In the method and apparatus disclosed in Ramesh, a received decoded signal is decoded by an electrical circuit that is disposed in accordance with a so-called butterfly structure. The Ramesh procedure is used exclusively for channel decoding of channel-coded signals.--.

Replace the paragraphs beginning on lines 1, 11, 16, 18, and 23 of page 2, with:

--W. Koch and A. Baier, Optimum and Suboptimum Detection of Coded Data Disturbed by Time-Varying Intersymbol Interference, IEEE GLOBECOM, pages 1679 - 1684, 1999 (hereinafter "Koch"), discloses the determination of a so-called transition metric for a Viterbi algorithm in the course of equalization of physical signals for so-called soft decision equalization. Furthermore, Koch discloses the entire Viterbi method, matched to the appropriate transition metrics for a so-called butterfly structure of a trellis, and the determination of the "optimum" signal sequence of the received signals by so-called back-tracing from the optimum trellis determined.

One particular disadvantage of the procedure described in Koch is that the circuit described there is suitable only for

equalization of received physical signals. The Koch apparatus cannot be used for channel decoding of physical signals.

The principles of the Viterbi algorithm are described in G.D. Forney, The Viterbi-Algorithm, Proceedings of the IEEE, Vol., 61, No. 3, pages 268 - 278, 1973 (hereinafter "Forney").

Summary of the Invention:

It is accordingly an object of the invention to provide a device and method to carry out a veterbi algorithm that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices of this general type and that makes it possible to use a Viterbi algorithm flexibly for different, selectable operating modes, for example, for equalization and for decoding received physical signals.--

Replace the paragraphs beginning on page 12, lines 5, 7, 9, 12, 15, 20, and 24 with:

--Brief Description of the Drawings:

Fig. 1 is a block circuit diagram of an exemplary embodiment of an electrical circuit according to the invention;

Fig. 2 is a block circuit diagram illustrating the sending, transmission, and reception of an electrical signal;

Fig. 3A is a diagram illustrating a binary trellis according to a butterfly structure for equalization of an electrical signal;

Figs. 3B is a diagram illustrating a binary trellis according to a butterfly structure for decoding an electrical signal; and

Fig. 4 is a block circuit diagram of an exemplary embodiment of a digital signal processor according to the invention.

Description of the Preferred Embodiments:

Referring now to the figures of the drawings in detail and first, particularly to Fig. 2 thereof, there is shown, symbolically, a source 201, from which a message 202 is intended to be transmitted from a transmitter 200 to a sink 221 in a receiver 211.--.

Replace the paragraphs beginning on page 17, line 14, with:

--To simplify understanding of the invention, the rough structure of the Viterbi algorithm will be explained in the following text (see Figure 3A and Figure 3B). Details of the Viterbi algorithm are described in Fourny.--.